SDRAM
Serial Presence Detect (SPD) Data Structure
(168- and SO-144 DIMM)

Intel Specification

REVISION 1.1

Changes:

Revision 1.1 adds comments to clarify several Bytes:

Bytes 3-4: Note added to clarify address row/column 1/16 rollup useage.
Bytes 5,17: Note added to clarify Module, SDRAM Device bank useage.
Bytes 23-26: Note added to clarify timing1/16ns rollup useage.

Revision 1.0 adds/corrects/clarifies to achieve Jedec consistency for existing SDRAM SPD specified in 168-DIMM and SO-144 specs.

Note: This specification is a modification of the SPD version extracted from "4-clock, unbuffered 168-pin SDRAM DIMM" Rev 1.0, authored by Andrew McRonald.

This document releases the first stand-alone Intel EDO/SDRAM SPD document.

Changes from previous (a) *2-clock* "66Mhz 64-bit Unbuffered SDRAM DIMM Specification revision 1.2" , (b) 4-clock "64-bit Unbuffered SDRAM DIMM Specification " and (c) "SO-144" include:

Bytes 3 and 4: # of Row and Col Addresses:
Single-sized SDRAM devices (all same) use lower nibble
Mixed-sized SDRAM devices (Bank 2) use upper nibble
Redundant bit moved to Module Attributes Byte 21, bit 6.
Bytes 9 and 10: SDRAM Min Cycletime and Access time from clock:
Both now specify highest CAS Latency (ie, CL3, 4, ...)
Byte 21: SDRAM Module Attributes:
Redundant Row Address bit moved from B3-b7 to B21-b6.
SDRAM Timings:
Byte 23: Add Min Clock Cycletime for 2nd highest CAS Lat (CL x-2)
Byte 24: Add Max Data Access from Clock for 2nd highest CAS Lat
Byte 25: Add Min Clock Cycletime for 3rd highest CAS Lat (CL x-3)
Byte 26: Add Max Data Access from Clock for 3rd highest CAS Lat
Byte 27: Add Minimum Row Precharge time (Trp)
Byte 28: Add Minimum Row Active to Row Active Delay (Trrd)
Byte 29: Add Minimum RAS to CAS Delay (Trcd)
Byte 30: Add Minimum Activate to Precharge Delay (Tras)
Byte 31: Add Mixed- and Single-Size Module ***Bank Density***.
Size of Memory bank shown by 1 in appropriate size bit(s). Two 1's indicate mixed 2-bank, single 1 indicates size per bank, non-mix.

EEPROM Component Specification:
Vol in **EEPROM AC and DC Characteristics** changed to 0.4V *@ 3.0 mA*.

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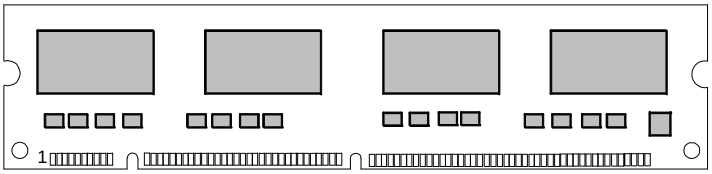
1.0 Introduction

This specification defines the Serial Presence Detect (SPD) electrical and Data Structure requirements for Synchronous DRAM Dual In-Line Memory Modules (SDRAM DIMMs) and Small-outline Memory Modules (SO-DIMM). These SDRAM DIMMs are intended for use as main memory installed on personal computer, ***work-station, and/or server*** motherboards.



168-DIMM reference

This specification largely follows the JEDEC defined 168-pin and SO-144 SDRAM DIMM SPD specs as of July 1996. *Changes in process are currently shown in italics.*

2.0 SDRAM Module Performance Grades

Three performance grades are defined in the SPD matrix:

CAS Latency x	highest latency, lowest performance
CAS Latency x-1	2nd highest latency
CAS Latency x-2	3rd highest latency, highest performance (may restrict freq)

This is a relative series of three latencies, CL x being the most commonly available at this speed grade. The performance grade of the module is determined by the read data access time (Tac), and RAS cycle time (Trc) supported by the SDRAM components.

Latency numbers in the sequence will depend on the speeds which are supported by the module.

3.0 EEPROM Component Specifications

The Serial Presence Detect function is implemented using a 2048 bit EEPROM component. This nonvolatile storage device contains data programmed by the DIMM manufacturer that identifies the module type and various SDRAM organization and timing parameters. System read/write operations to the EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0) which provide the EEPROM Device Address. If the EEPROM device has a Write Protect input pin, it must be tied in the non-write protect state on the DIMM PCB. The EEPROM device selected by the DIMM manufacturer must use the SA(2:0) device address signals. The EEPROM must operate with a V_{CC} of 3.0 Vdc to 3.6 Vdc.

Table 1: EEPROM Component Absolute Maximum Ratings

Parameter	Range
All Input or Output Voltages with Respect to Ground	+4.6V to -0.3V
Ambient Storage Temperature	-40 °C to +100 °C

Table2: EEPROM Component Operating Conditions

Parameter	Range
Ambient Operating Temperature	0 °C to +70 °C
Positive Power Supply	3.0V to 3.6V

Table 3: EEPROM Component A.C. and D.C. Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		5.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		100	uA
I_{LI}	Input Leakage Current	V_{IN} = GND or V_{CC}		10	uA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		10	uA
V_{IL}	Input Low Voltage		-0.3	V_{CC} X 0.3	V
V_{IH}	Input High Voltage		V_{CC} X 0.7		V
V_{OL}	Output Low Voltage	I_{OL} = *3.0 mA*		0.4	V

Table 4: EEPROM Component A.C. Timing Parameters

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Supression Time Constant at SCL, SDA inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	us
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		us
$t_{HD:STA}$	Start Condition Hold Time	4.5		us
t_{LOW}	Clock Low Time	6.7		us
t_{HIGH}	Clock High Time	4.5		us
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		us
$t_{HD:DAT}$	Data In Hold Time	0		us
$t_{SU:DAT}$	Data In Setup Time	500	1	ns
t_R	SDA and SCL Rise Time		1	us
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		us
t_{DH}	Data Out Hold Time	300		ns
t_{WR}	Write Cycle Time		15	ms

Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the write cycle, the EEPROM bus interface circuits are disabled, SDA remains high due to pull-up resistor, and the EEPROM does not respond to its slave address.

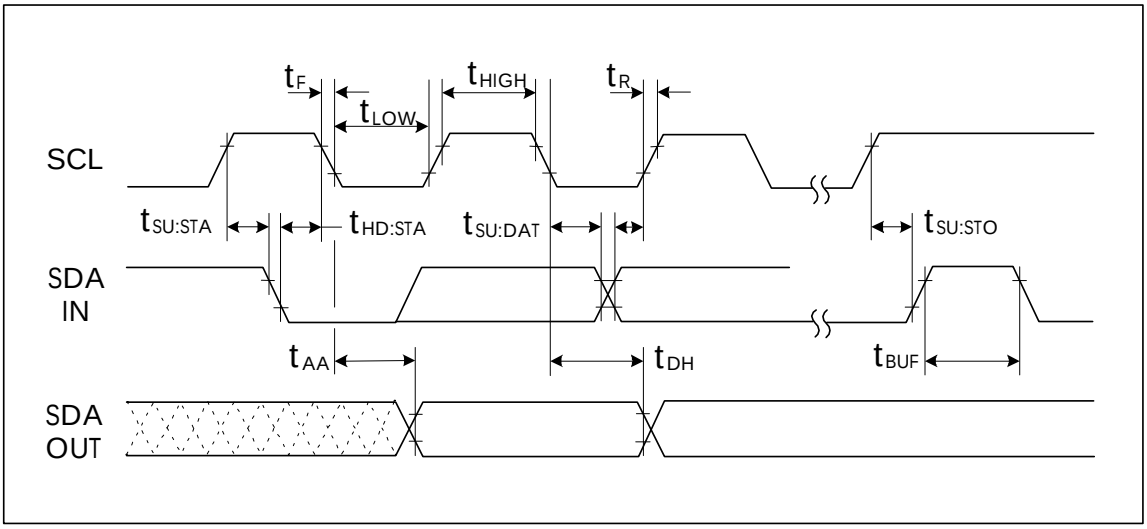


Figure 2: EEPROM Component A.C. Timing Parameters

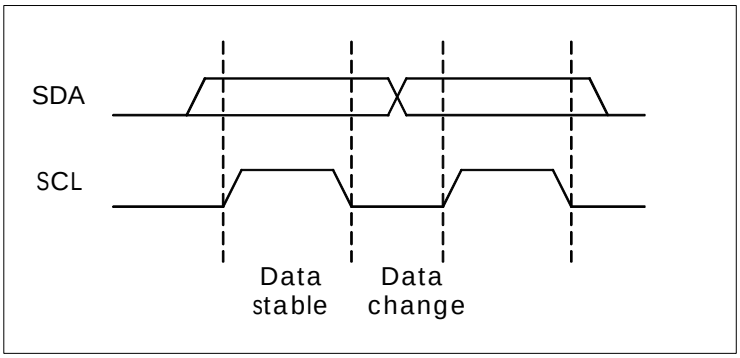


Figure 3: EEPROM Data Validity

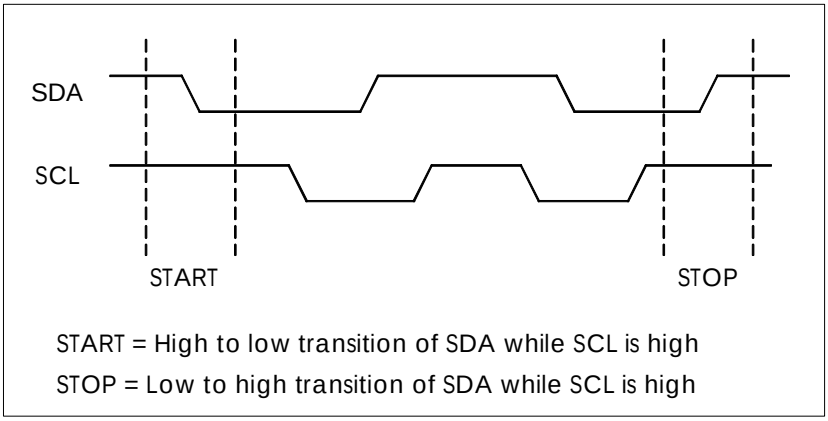


Figure 4: EEPROM Start and Stop conditions

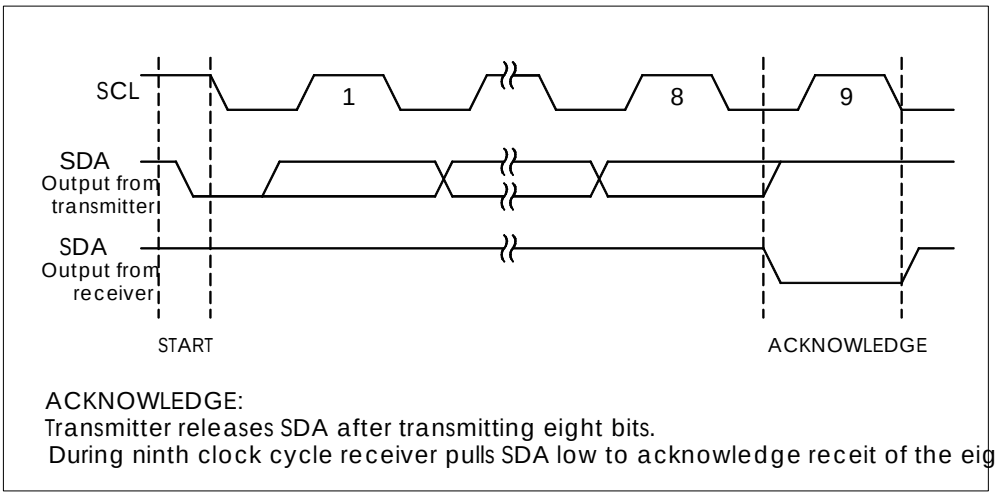


Figure 5: EEPROM Acknowledge

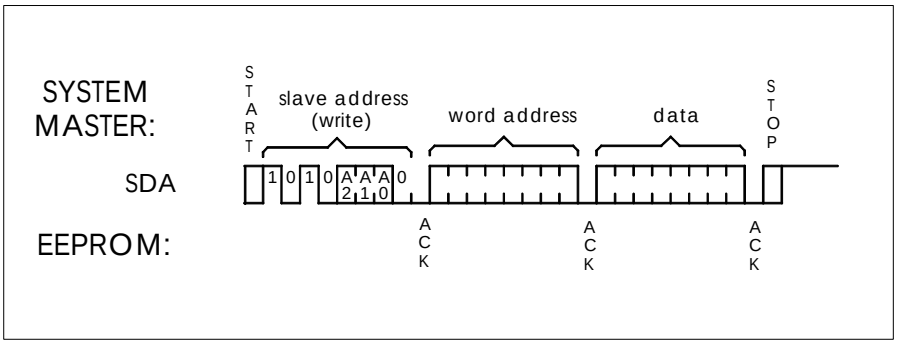


Figure 6: EEPROM Byte Write Operation

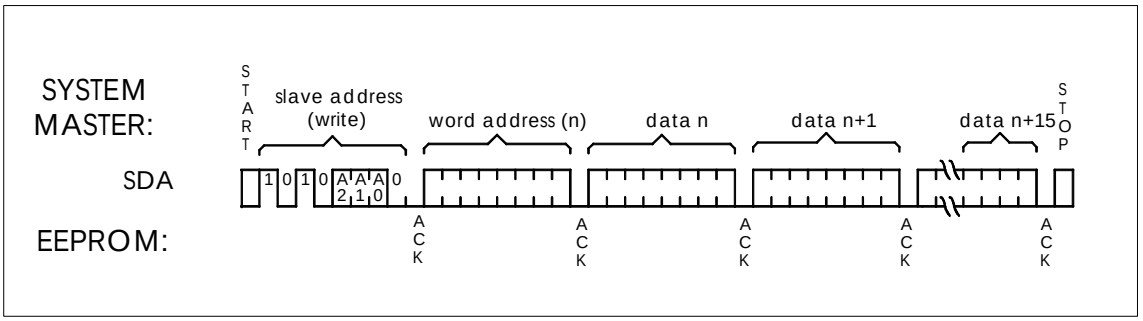


Figure 7: EEPROM Page Write Operation

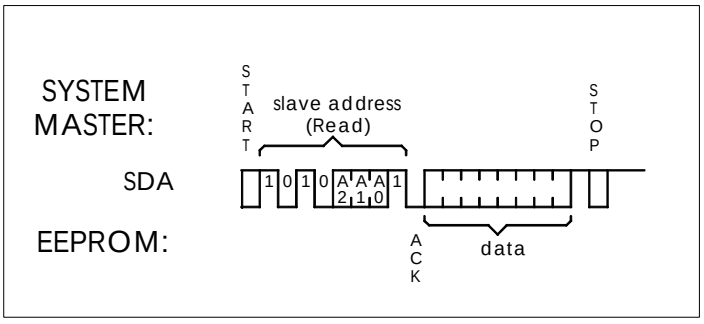


Figure 8: EEPROM Current Address Read Operation

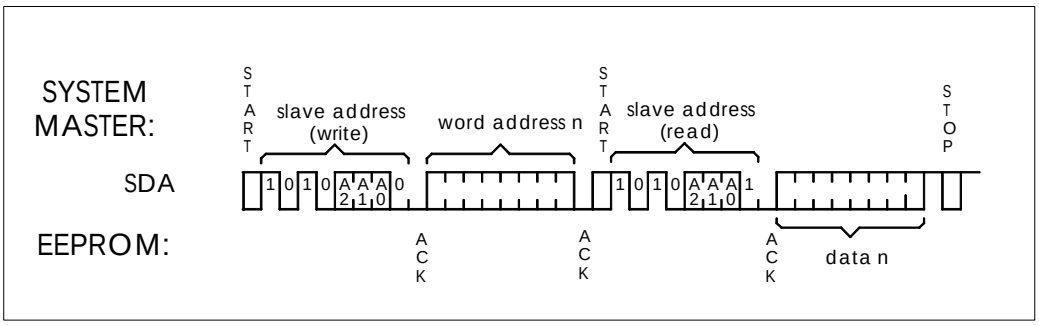


Figure 9: EEPROM Random Read Operation

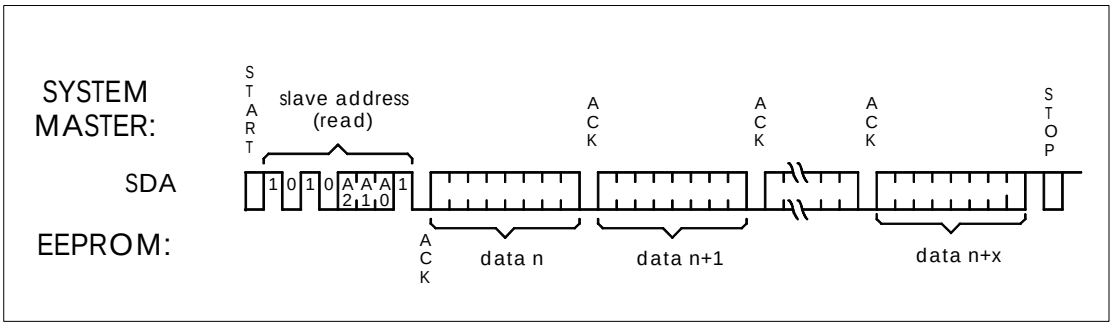


Figure 10: EEPROM Sequential Read Operation

4.0 Serial Presence Detect EEPROM Data

Table 5: Serial Presence Detect Data Format

Byte Number	Function	Required/ Optional
0	Defines # of bytes written into serial memory at module manufacturer	Required
1	Total # of bytes of SPD memory device	Required
2	Fundamental memory type (FPM, EDO, SDRAM..) *from Appendix A*	Required
3	# of row addresses on this assembly *(includes Mixed-size Row addr)*	Required
4	# Column Addresses on this assembly *(includes Mixed-size Col addr)*	Required
5	# Module Banks on this assembly	Required
6	Data Width of this assembly	Required
7	... Data Width continuation	Required
8	Voltage interface standard of this assembly	Required
9	SDRAM Cycle time***, CL=X*** (highest CAS latency)	Required
10	SDRAM Access from Clock (highest CAS latency)	Required
11	DIMM Configuration type (non-parity, ECC)	Required
12	Refresh Rate/Type	Required
13	*Primary SDRAM Width*	Required
14	*Error Checking SDRAM width*	Required
15	Minimum Clock Delay Back to Back Random Column Address	**Required***
16	Burst Lengths Supported	**Required***
17	# of Banks on Each SDRAM Device	**Required***
18	CAS# Latencies Supported	**Required***
19	CS# Latency	**Required***
20	Write Latency	**Required***
21	*SDRAM Module Attributes*	**Required***
22	*SDRAM Device Attributes: General*	**Required***
23	*Min SDRAM Cycle time at **CL X-1** (2nd highest CAS latency)*	**Required***
24	*SDRAM Access from Clock at **CL X-1** (2nd highest CAS latency)*	**Required***
25	*Min SDRAM Cycle time at **CL X-2** (3rd highest CAS latency)*	**Optional***
26	*Max SDRAM Access from Clock at **CL X-2** (3nd highest CAS latency)*	**Optional***
27	*Min Row Precharge Time (Trp)*	**Required***
28	*Min Row Active to Row Active (Trrd)*	**Required***
29	*Min RAS to CAS Delay (Trcd)*	**Required***
30	*Minimum RAS Pulse Width (Tras)*	**Required***
31	*Density of each bank on module (mixed, non-mixed sizes)*	Required
32-61	Superset Information (may be used in future)	
62	SPD Data Revision Code	Required
63	Checksum for bytes 0-62	Required
64-71	Manufacturer's JEDEC ID code per JEP-108E	Optional
72	Manufacturing Location	Optional
73-90	Manufacturer's Part Number	Optional
91-92	Revision Code	Optional
93-94	Manufacturing Date	Optional
95-98	Assembly Serial Number	Optional
99-125	Manufacturer Specific Data	Optional
126	Intel specification frequency	Required
127	Intel Specification CAS# Latency support	Required
128+	Unused storage locations	

Notes: **Required/Optional*** (bold*) are SDRAM only bytes

Byte 0 - Number of Bytes used by Module Manufacturer (General)

This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number of bytes	Hex Value
Undefined	00
1	01
2	02
3	03
.	.
128	80
.	
254	FE
255	FF

Byte 1 - Total SPD Memory Size (General)

This field describes the total size of the serial memory used to hold the Serial Presence Detect data.

Serial Memory Size	Hex Value
RFU	00
2 Bytes	01
4 Bytes	02
8 Bytes	03
16 Bytes	04
32 Bytes	05
64 Bytes	06
128 Bytes	07
256 Bytes	08
512 Bytes	09
1024 Bytes	0A
2048 Bytes	0B
4096 Bytes	0C
8192 Bytes	0D

Byte 2 - Memory Type (General)

This field describes the fundamental memory type implemented on the module.

Memory Type	Hex Value
EDO	02
SDRAM	04
.	.

Note for Bytes 3-4: Bytes 3-4 show a roll-up value for Hex 1, 2, 3 (i.e., 1row/16rows). For SDRAM devices over duration of REV 1 in Byte 62 (SPD Jedec Rev level), values of 1-3rows/cols are not expected, and Hex equivalent is 16-18rows/columns. Jedec Byte 62 would change rev level if values of 1-3 row/col become available.

Byte 3 - Number of Row Address Bits (SDRAM specific)

This field describes the number of row address bits in the SDRAM array. Note: the number of row address bits does not include the bank selects (BA0, BA1). If the module has only one bank OR if the module has two banks of the same size and organization, then bits 3:0 describe the number of row address bits, and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the row addressing for bank 1 and bits 7:4 decribe the row addressing for bank 2.

Number of Row Addr bits	Bits 3:0 Hex Value
Undefined	0
1/16	1
2/17	2
.	.
7	7
8	8
9	9
10	A
11	B
.	.
14	E
15	F

Number of Row Addr bits	Bits 7:4 Hex Value
Undefined	0
1/16	1
2/17	2
.	.
7	7
8	8
9	9
10	A
11	B
.	.
14	E
15	F

BYTE 4 - Number of Column Address Bits (SDRAM specific)

This field describes the number of column address bits in the SDRAM array. Note: the number of column address bits does not include the bank selects (BA0, BA1), or the AutoPrecharge bit. If the module has only one bank OR if the module has two banks of the same size and organization, then bits 3:0 describe the number of column address bits, and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the column addressing for bank 1 and bits 7:4 decribe the column addressing for bank 2.

Number of Col Addr bits	Bits 3:0 Hex Value
Undefined	0
1/16	1
2/17	2
.	.
7	7
8	8
9	9
10	A
11	B
12	C
13	D
14	E
15	F

Number of Col Addr bits	Bits 7:4 Hex Value
Undefined	0
1/16	1
2/17	2
.	.
7	7
8	8
9	9
10	A
11	B
12	C
13	D
14	E
15	F

BYTE 5 - Number of Module Banks

This field describes the number of banks of SDRAM components on the module. Applies to module banks only, while Byte 17 applies to SDRAM device banks (a module with 2 Banks could have devices with 2-16 internal banks).

Number of Banks	Hex Value
Undefined	00
1	01
2	02
3	03
.	.
254	FE
255	FF

BYTES 6 & 7 - Module Data Width

This field describes the data width on the SDRAM module. Bit 0 of byte 6 is the LSB and Bit 7 of byte 7 is the MSB.

Module Data Width	Byte 7 (Hex)	Byte 6 (Hex)
Undefined	00	00
1	00	01
2	00	02
3	00	03
.	.	.
32	00	20
.		.
36	00	24
.	.	.
64	00	40
.	.	.
72	00	48
.	.	.
80	00	50
.		.
128	00	80
.	.	.
144	00	90
.	.	.
160	00	A0
.	.	
256	01	00.

BYTE 8 - Module Interface Signal Levels

This field describes the SDRAM module signal voltage interface.

Voltage Interface	Hex Value
5.0 Volt/TTL	00
LVTTL	01
HSTL 1.5	02
SSTL 3.3	03
SSTL 2.5	04
TBD	05
TBD	06
.	.
New Table	FF

BYTE 9 - SDRAM Cycle time (highest CAS latency)

This field defines the total minimum cycle time (clock period) for the SDRAM. For example if the SDRAMs support CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines Tclk for CAS latency 3. The byte is broken into two nibbles: the high order nibble (bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the low order nibble has a granularity of 1/10 ns and is added to the value of the higher nibble.

BYTE 10 - SDRAM Access time from Clock (highest CAS latency)

This field defines the maximum clock to data out for the SDRAM (Tac). For example if the SDRAMs support CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines Tac for CAS latency 3. The byte is broken into two nibbles: the high order nibble (bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the low order nibble has a granularity of 1/10 ns and is added to the value of the higher nibble.

BYTE 11 - Module Configuration Type

This field defines the module's error detection and correction scheme.

Error Detect/Correct	Hex Value
None	00
Parity	01
ECC	02
TBD	03
TBD	04
TBD	05
TBD	06
.	.
TBD	FF

BYTE 12 - Refresh Rate/Type

This field defines the module's refresh rate and type.

Refresh Period	Bit 7, Self Refresh Flag	Bits 6-0 (hex)
Normal (15.625 us)	0	00
Reduced (.25x)...3.9 us	0	01
Reduced (.5x) 7.8 us	0	02
Extended (2x) 31.3 us	0	03
Extended (4x) 62.5 us	0	04
Extended (8x) 125 us	0	05
TBD	0	06
TBD	0	07
TBD	0	08
TBD	0	09
.	.	.
Self Refresh		
Normal (15.625 us)	1	00
Reduced (.25x)...3.9 us	1	01
Reduced (.5x) 7.8 us	1	02
Extended (2x) 31.3 us	1	03
Extended (4x) 62.5 us	1	04
Extended (8x) 125 us	1	05
TBD	1	06
TBD	.	.
TBD	.	.
.	.	.
TBD	1	7F

BYTE 13 - SDRAM Width (Primary SDRAM)

Bits 6:0 of this byte define the data width of the primary SDRAM components used on the module. The primary SDRAM is that which is used for data. Examples of primary (data) SDRAM widths are x4, x8, x16, x32. Bit 7 of this byte is a flag which indicates that a 2nd bank on the module has a primary SDRAM width of 2X that of the first bank. If the module has two banks with the same Primary SDRAM width, then bit 7 remains as "0".

Primary SDRAM Component Data Width	Bits 6:0 Hex Value
Undefined	00
1	01
2	02
3	03
4	04
.	.
8	08
.	.
16	10
.	.
32	20
.	.
127	7F

Bank Configuration	Bits 7 Value
No Bank 2 -OR- Bank 2 uses same width Primary SDRAM as Bank 1	0
Bank 2 Primary SDRAM is 2X the width of Bank 1	1

BYTE 14 - Error Checking SDRAM Width

If the module incorporates error checking and if the primary data SDRAM does not include these bits; i.e. there are separate error checking SDRAMs, then the error checking SDRAM's width is expressed in this byte. Examples of error checking SDRAM widths include x4, x8, x16.

Bits 6:0 of this byte define the data width of the Error Checking SDRAM components used on the module. Bit 7 is a flag which indicates that a 2nd bank on the module has Error Checking SDRAM width. of 2X that of the first bank. If the module has two banks with the same Error Checking SDRAM width, then bit 7 remains as "0".

Error Checking SDRAM Component Data Width	Bits 6:0 Hex Value
Undefined	00
1	01
2	02
3	03
4	04
5	05
6	06
7	07
8	08
.	.
16	10
.	.
32	20
.	.
127	7F

Bank Configuration	Bits 7 Value
No Bank 2 -OR- Bank 2 uses same width EC SDRAM as Bank 1	0
Bank 2 EC SDRAM is 2X the width of Bank 1	1

BYTE 15 - SDRAM Device Attributes, Min Clock Delay for Back to Back Random Column Addresses

Number of Clocks	Hex Value
Undefined	00
1	01
2	02
3	03
4	04
5	05
6	06
.	.
255	FF

BYTE 16 - SDRAM Device Attributes, Burst Lengths Supported

This byte defines various burst lengths supported. If the burst length is supported, then the corresponding bit is "1"

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Burst Length = Page	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	Burst Length = 2	Burst Length = 1
1 or 0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

BYTE 17 - SDRAM Device Attributes, Number of Banks on SDRAM Device

This byte defines the number of banks internal to the SDRAM devices. Applies to device banks only, while Byte 5 applies to Module banks (a module with 2 Banks could have devices with 2-16 internal banks).

Number of Device Banks	Hex Value
Undefined	00
1	01
2	02
3	03
4	04
5	05
.	.
255	FF

BYTE 18 - SDRAM Device Attributes, CAS Latency

This byte defines which CAS latencies are supported. If the bit is "1" then that CAS Latency is supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CAS Latency = 7	CAS Latency = 6	CAS Latency = 5	CAS Latency = 4	CAS Latency = 3	CAS Latency = 2	CAS Latency = 1
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

BYTE 19 - SDRAM Device Attributes, CS Latency

This byte defines which CS latencies are acceptable for the Module. If the bit is "1" then that CS Latency is supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CS Latency = 6	CS Latency = 5	CS Latency = 4	CS Latency = 3	CS Latency = 2	CS Latency = 1	CS Latency = 0
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

BYTE 20 - SDRAM Device Attributes, WE Latency

This byte defines which CS latencies are acceptable for the Module. If the bit is "1" then that WE Latency is supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	WE Latency = 6	WE Latency = 5	WE Latency = 4	WE Latency = 3	WE Latency = 2	WE Latency = 1	WE Latency = 0
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

BYTE 21 - SDRAM Module Attributes

This byte defines various aspects of the module. If the aspect is TRUE, then the corresponding bit is "1".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	***Redundant Row Addr***	Differential Clock Input	Registered DQMB Inputs	Buffered DQMB Inputs	On-Card PLL (Clock)	Registered Address/ Control Inputs *	Buffered Address/ Control Inputs *
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

* Address, RAS, CAS, WE, CKE, S

** Redundant addressing implies the use of SDRAMs having the same address depth (e.g. 4Mx4 mixed with 4Mx16) in the same 8-byte quad word, but having different RAS/CAS addressing and/or different numbers of device banks. Actual implementation is not yet determined.

BYTE 22 - SDRAM Device Attributes, General

This byte defines various aspects of the SDRAMs on the module. If the aspect is TRUE, then the corresponding bit is "1".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	Upper Vcc tolerance: 0 = 10% 1 = 5%	Lower Vcc tolerance: 0 = 10% 1 = 5%	Supports Write1/Read Burst	Supports Precharge All	Supports Auto-Precharge	Supports Early RAS# Precharge
0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Vcc Tolerance refers to the voltage range under which the SDRAMs operate to the timings specified in the SPD bytes 9, 10, 23-30.

Note for Bytes 23-26: Bytes 23-26 show a roll-up value for Hex 1, 2, 3 (i.e., 1ns/16ns). For SDRAM devices over duration of REV 1 in Byte 62 (SPD Jedec Rev level), values of 1-3ns are not expected, and Hex equivalent is 16-18ns. Jedec Byte 62 will change rev level when values of 1-3 ns become available.

BYTE 23 - SDRAM Cycle time (2nd highest CAS latency)

This field defines the minimum cycle time (clock period) for the SDRAM when operating at its 2nd highest CAS latency. For example if the SDRAMs support CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines Tclk for CAS latency 2. The byte is broken into two nibbles: the high order nibble (bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the low order nibble has a granularity of 1/10 ns and is added to the value of the higher nibble.

Nanoseconds	Bits 7-4 Hex Value
Undefined	0
1ns / 16ns	1
2ns / 17ns	2
3ns / 18 ns	3
4	4
.	.
15	F

1/10 nanoseconds	Bits 3-0 Hex Value
0	0
1	1
2	2
3	3
4	4
.	.
9	9

BYTE 24 - SDRAM Access from Clock (2nd highest CAS latency)

This field defines the maximum clock to data out for the SDRAM (Tac) when operating at its 2nd highest CAS latency. For example if the SDRAMs support CAS latency of 3, 2 and 1(as indicated in byte 18), this byte defines Tac for CAS latency 2. The byte is broken into two nibbles: the high order nibble (bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the low order nibble has a granularity of 1/10 ns and is added to the value of the higher nibble.

Nanoseconds	Bits 7-4 Hex Value
Undefined	0
1ns / 16ns	1
2ns / 17ns	2
3ns / 18 ns	3
4	4
.	.
15	F

1/10 nanoseconds	Bits 3-0 Hex Value
0	0
1	1
2	2
3	3
4	4
.	.
9	9

BYTE 25 - SDRAM Cycle time (3rd highest CAS latency)

This field defines the minimum cycle time (clock period) for the SDRAM when operating at its 3rd highest CAS latency. For example if the SDRAMs support CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines Tclk for CAS latency 1. The byte is broken into two sections: the 6 high order bits (bits 7:2) designate the cycle time to a granularity of 1 ns; the value presented by bits 1:0 has a granularity of 1/4 ns and is added to the value of the higher nibble.

Nanoseconds	Bits 7-2 Binary Value
Undefined	000000
1ns / 16ns	000001
2ns / 17ns	000010
3ns / 18 ns	000011
4	000100
.	.
15	111111

1/4 nanoseconds	Bits 1-0 binary value
0	00
1	01
2	10
3	11

BYTE 26 - SDRAM Access from Clock (3rd highest CAS latency)

This field defines the maximum clock to data out for the SDRAMs (Tac) when operated at its 3rd highest CAS latency. For example if the SDRAMs support CAS latency of 3, 2 and 1(as indicated in byte 18), this byte defines Tac for CAS latency 1. The byte is broken into two sections: the 6 high order bits (bits 7:2) designate the access time to a granularity of 1 ns; the value presented by bits 1:0 has a granularity of 1/4 ns and is added to the value of the higher nibble.

Nanoseconds	Bits 7-2 Binary Value
Undefined	000000
1ns / 16ns	000001
2ns / 17ns	000010
3ns / 18 ns	000011
4	000100
.	.
15	111111

1/4 nanoseconds	Bits 1-0 Binary Value
0	00
1	01
2	10
3	11

BYTE 27 - Minimum Row Precharge Time

This byte defines the precharge to activate minimum (Trp) using 1ns granularity.

Precharge Minimum	Bits 7-0 Hex Value
undefined	00
1 ns	01
2 ns	02
.	.
30 ns	1E
.	.
45 ns	2D
.	.
255 ns	FF

BYTE 28 - Row Active to Row Active Min

This byte defines the minimum row activate to row activate delay (Trrd) using 1 ns granularity.

Act to Act Minimum	Bits 7-0 Hex Value
undefined	0
1 ns	1
2 ns	2
.	.
30 ns	1E
.	.
45 ns	2D
.	.
255 ns	FF

BYTE 29 - RAS to CAS Delay Min

This byte defines the minimum RAS to CAS delay (Trcd) using 1ns granularity.

RAS to CAS Delay Minimum	Bits 7-0 Hex Value
undefined	0
1 ns	1
2 ns	2
.	.
30 ns	1E
.	.
45 ns	2D
.	.
255 ns	FF

BYTE 30 - Minimum RAS Pulse Width

This byte defines the minimum activate to precharge time (Tras) using 1 ns granularity.

Activate to Precharge Minimum	Bits 7-0 Hex Value
undefined	0
1 ns	1
2 ns	2
.	.
60 ns	3C
.	.
75 ns	4B
.	.
90 ns	5A
.	.
255 ns	FF

BYTE 31 - Density of Each Bank on Module

This byte describes the memory capacity of each physical bank on the DIMM module.. This byte will have at least one bit set to a "1" to represent at least one bank's size. If there is more than one bank on the module (as represented in Byte 5) and they have the same size, then only one bit in this field is set. If the module has more than one bank of different sizes then more than one bit will be set. For example:

# Banks	Size of Bank 1	Size of Bank 2	Byte 31 contents
1	32MByte	N/A	0000 1000
2	32MByte	32MByte	0000 1000
2	32MByte	16MByte	0000 1100

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Size	512MByte	256MByte	128MByte	64MByte	32MByte	16MByte	8MByte	4MByte
N/Y	0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

BYTE 62 - SPD Data Revision Code

This byte indentifies the JEDEC SDRAM DIMM SPD Data revision to which the module conforms.

SPD Revision	Bits 7-0 Hex Value
Current Release Dec 96	01
.	.

BYTE 63 - Checksum for Bytes 0-62

This byte is the checksum for bytes 0 through 62. This byte contains the value of the low 8-bits of the arithmetic sum of bytes 0 through 62.

BYTES 64-71 - Manufacturer's JEDEC ID Code

BYTE 72 - Manufacturing Location

BYTE 73-90 - Manufacturer's Part Number

BYTE 91-92 - Revision Code

BYTE 93-94 - Manufacturing Date

BYTE 95-98 - Assembly Serial Number

BYTE 99-125 - Manufacturer Specific Data

BYTE 126 - Intel specification frequency

This byte defines the clock frequency of the Intel SDRAM DIMM specification.

Intel Specification Frequency	Hex Value
66 Mhz	66

This byte is required for compatability with previously released systems.

BYTE 127 - Intel specification CAS# Latency Support

This byte defines the SDRAM component CAS# Latency modes that conform to the Intel SDRAM DIMM specification AC timings.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	TBD	CAS Latency = 3	CAS Latency = 2	TBD
0	0	0	0	0	1 or 0	1 or 0	0

Performance Grade	Hex Value
CAS Latency 3	04
CAS Latency 2 (Restricted)	06
CAS Latency 2	06

This byte is required for compatability with previously released systems.